Amendments to the Drawings:

The attached "new sheets" of drawings include changes to Figs. 3, 4 and 5 only. These sheets, which include Figs. 1-5, replace the original sheets including Figs. 1-5. In Figs. 3, 4 and 5, minor informalities have been corrected.

Attachment: New Sheets of drawings

REMARKS

Claims 1-16 are pending. By this amendment, claims 1, 2, 6, 7, 9, 10, 14, and 15 are amended, new claim 17 is added, and claims 5 and 13 are cancelled. Support for the claim amendments and new claim can be found at least in original claims 5 and 13 and at page 9, lines 17-22 of the specification. No new matter is introduced. Reconsideration and issuance of a Notice of Allowance are respectfully requested.

Drawing Objection

The drawings are objected to because of informalities. The drawings have been amended to remove the informalities. Withdrawal of the drawing objection is respectfully requested.

Double Patenting Rejection

Claims 1-16 are provisionally rejected based on the non-statutory obviousness-type double patenting as being unpatentable over claims 1-20 of co-pending Application No. 10/853,518. Filed herewith is a terminal disclaimer in accordance with 37 C.F.R. §1.321 disclaiming any term extending beyond that of the '518 co-pending application. Withdrawal of the rejection of the claims based on the judicially created doctrine of double patenting is respectfully requested.

Claim Rejections Under 35 U.S.C. §112

Claims 1, 2, 3, 10, and 11 are rejected under 35 U.S.C. § 112, second paragraph. Claims 1, 2, and 10 have been amended to correct the minor informalities. Withdrawal of the rejections under 35 U.S.C. § 112 is respectfully requested.

Claim Rejections Under 35 U.S.C. §101

Claims 9-16 are rejected under 35 U.S.C. § 101 for directing to non-statutory subject matter. Specifically, the Office Action asserts on page 4 that the claims merely involve calculations and manipulations of data in performing computations, and does not result in a physical change in the computer structure or result in any physical transformation. This rejection is respectfully traversed.

The present application eliminates an entire carry-save adder (CSA) and reduces propagation delays within a circuit for performing a floating point multiply-accumulate operation (FMAC), resulting in an increased speed of calculation for the FMAC operation. (See the Summary section of the present application.) The method for eliminating the CSA, which obviously provides a practical application, may be implemented using a computer. Therefore,

method claims 9-16 are directed to statutory subject matter. Withdrawal of the rejections of claims 9-16 under 35 U.S.C. § 101 is respectfully requested.

Claim Rejections Under 35 U.S.C. §103

Claims 1-5, 7-13, 15 and 16 are rejected under 35 U.S.C. § 103(a) over U.S. Patent 5,790,444 to Olson et al. (hereafter Olson). Specifically, the Office Action asserts that "Olson et. al. discloses in figure 3 an apparatus for generating a shift for use in a floating point multiply accumulate operation. The apparatus clearly has a carry-save adder (26) and a logic block (34) for performing a carry-lookahead add operation to produce a sum as claimed." While acknowledging that Olson does not specifically disclose the logic block having a logic circuit for performing an XOR logic operation, the Office Action asserts that "since it is well-known in the art that in a carry-lookahead adder sums Si are computed in parallel and equal to Pi XOR Ci, a person of ordinary skill in the art would have found it obvious to provide the carry-lookahead adder (34) of Olson el al. with logic circuits for performing XOR logic operations on Pi and Ci in order to obtain the sums Si, wherein one of Pi and Ci is seen as a second result and the other as a control signal as claimed." This rejection is respectfully traversed.

Olson is directed to a fast alignment unit for multiply-add floating point unit. Figure 3 of Olson merely shows a shift amount generator including, among other components, a carry save adder 26 and carry look-ahead adder 34. However, neither Figure 3 nor the corresponding text discloses or suggests performing an exclusive-OR logic operation between a most significant bit of the second result and the control signal to produce a value for use in the floating point multiply-accumulate operation. Applicant respectfully objects to the assertion that "a person of ordinary skill in the art would have found it obvious to provide the carry-lookahead adder (34) of Olson el al. with logic circuits for performing XOR logic operations on Pi and Ci in order to obtain the sums Si, wherein one of Pi and Ci is seen as a second result and the other as a control signal as claimed." Applicant respectfully requests that the Office Action provides a valid reference disclosing such a feature. Furthermore, even if an XOR logic operation is known in the art, no art in the record discloses or suggests the feature of performing an exclusive-OR logic operation between a most significant bit of the second result and the control signal.

The present application eliminates an entire carry-save adder (CSA) and reduces propagation delays within a circuit for performing a floating point multiply-accumulate operation

(FMAC), resulting in an increased speed of calculation for the FMAC operation. (See the Summary Section of the present application).

Referring to Figures 1-5 of the present application, the single carry-save adder and the modified carry-lookahead adder of Figure 2 produce the same result as the two carry-save adders and carry-lookahead adder of Figure 1 (prior art). The specification recites, at page 5, line 21 to page 6, line 3:

> The second CSA 20 can be eliminated based upon how the constant on line 22 operates. In particular, the second CSA 20 in circuit 10 uses only the lower eight bits of the constant on line 22, and those lower eight bits only vary in the most significant bit position. This variance is known because the FMAC operation uses a standard for operating on floating point numbers, as specified in IEEE Standard for Binary Floating-Point Arithmetic, IEEE Std. 754-1985, which is incorporated herein by reference.

Emphasis added.

Referring to Figure 4, which describes the modified carry-lookahead adder, the specification states that "the result of the stages, without use of a second CSA ... produces a SUMH signal 88 and its complement, a signal sSUMH 87", "operation of these stages, without use of a second CSA, produces a SUML signal 108 and its complement, a signal sSUML 107", and "the signals 87, 88, 107, and 108 produce the same resulting shift value on line 48 as the shift value produced on line 26 by signals 56, 58, 66, and 68." (See page 8, lines 9-10, 17-21 of the specification.)

Specifically, the difference between the circuit in Figure 4 and the circuit in Figure 3 (prior art) is the addition of the FETs controlled by the XORH/XORL signals. If an XOR operation is NOT going to be performed, the signal pair XORH/XORL will have values of 0/1. With these values, the circuit in Figure 4 will be exactly the same as the circuit in Figure 3. If an XOR operation is going to be performed, the signal pair XORH/XORL will have values of 1/0. In this case, the circuit in Figure 4 simply generates the inverse of what it generated in the prior case. Note that A XOR 1 is logically the same as taking the inverse of A.

Accordingly, the entire second carry-save adder (CSA) can be replaced by a single XOR logic operation, which is performed simultaneously with the carry-lookahead operation. The circuit in Figure 1 (prior art) performs two carry-save add operations and one carry-lookahead operation on the three values, while Figure 2 performs one carry-save add operation and combines an XOR logic operation with the carry-lookahead operation to produce the same result.

Amended claim 1 recites the above described novel features: "a carry-save adder ... that ... performs a carry-save add operation on the exponents of operands to produce a first result; a control circuit for generating a control signal; and a logic block ... performs a carry-lookahead add operation on the first result to produce a second result, the logic block having a logic circuit that performs an exclusive-OR logic operation between a most significant bit of the second result and the control signal to produce a value for use in the floating point multiply-accumulate operation," (emphasis added). As noted above, Olson does not disclose or suggest these features. Therefore, amended claim 1 is allowable.

Claims 2-4 and 7-8 are allowable at least because they depend from allowable claim 1 and for the additional features they recite.

Regarding independent claim 9, for at least the same reason as noted above with respect to claim 1, Olson does not disclose or suggest "performing a carry-save add operation on the exponents of operands to produce a first result; performing a carry-lookahead add operation on the first result to produce a second result; generating a control signal ... performing an exclusive-OR logic operation between a most significant bit of the second result and the control signal to produce a value for use in the floating point multiply-accumulate operation," as recited in amended claim 9 (emphasis added). Therefore, amended claim 9 is allowable.

Claims 10-12 and 15-16 are allowable at least because they depend from allowable claim 9 and for the additional features they recite.

Claims 6 and 14 are not rejected in the Office Action, and Applicant respectfully submits that claims 6 and 14 contain allowable subject matter. Claims 6 and 14 are written in independent form including all of the limitations of the base claim and any intervening claims. Allowance of claims 6 and 14 is respectfully requested.

New claim 17 recites the novel features of claim 1 and an additional feature: "the apparatus forms the floating point multiply-accumulate operation using a single carry-save adder (CSA)" (emphasis added). As noted above, this feature is not disclose or suggested by Olson. Therefore, new claim 17 is allowable.

In view of the above remarks, Applicant respectfully submits that the application is in condition for allowance. Prompt examination and allowance are respectfully requested.

Should the Examiner believe that anything further is desired in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

Date: **September 22, 2006**

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Attachment: New sheets of drawings